Flip Chip Packaging of a MEMS Neuro-Prosthetic System

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Abstract

A joint research team from California Institute of Technology and Jet Propulsion Laboratory is developing a fully miniaturized, smart implantable neuro-prosthetic system, by combining integrated electronics with Micro Electro Mechanical Structure (MEMS) based electrode arrays. The packaging group of this project team has been tasked with designing and fabricating a package to interface electrically between a MEMS electrode array, capable of extracting signals from brain, and an electronic chip, capable of providing on chip conditioning/processing of extracted data, while delivering the output data to a detector located outside the body. Area array flip chip technology will be used to attach the electronic chip and the MEMS device (10 x 10 array of fine 1 mm long, electrically isolated Si electrodes). Development efforts included evaluation of different interconnects, underbump metallizations, and underfills as well as optimization of soldering and coating parameters. Some specific challenges of the project include (1) handling of the MEMS array in a way that will allow reliable soldering of the fine 4 mil joints, without damaging the delicate structures and (2) selection of underfills and coatings capable of isolating the electronics from the body, while maintaining biocompatibility.

Keywords: flip chip, MEMS, neuro-prosthetic, soldering, biocompatibility

1. Introduction

During the past decade, MEMS based passive electrode arrays have been used to characterize the electrical signals of different regions of the brain. Such signals enable researchers to determine the source of thoughts contributing to body movements and may provide the foundation for the development of neuro-prosthetic devices capable of interfacing between the brain and a prosthetic limb (thereby providing optimum movement). The quality of signals extracted from the brain has unfortunately been limited, due to constraints attributed to the passive nature of the electrodes. A joint research team from California Institute of Technology and Jet Propulsion Laboratory is investigating the possibility of enhancing the quality of signals extracted from the brain by developing a fully miniaturized, smart implantable neuro-prosthetic system, which combines integrated electronics and a MEMS based electrode array.

The objective of the packaging team has been to design and fabricate a package to interface electrically between a commercially available, passive MEMS electrode array (Figure 1) and an electronic chip, while delivering the data to a detector located outside the body. The electrode array, which is capable of extracting signals from the brain, consists of a 10 x 10 array of fine 1 mm long, electrically isolated Si electrodes (Figure 2). The electronic chip attached to the array will be capable of providing on chip conditioning/processing of the extracted data, while simultaneously measuring the temperature of the surrounding tissue.

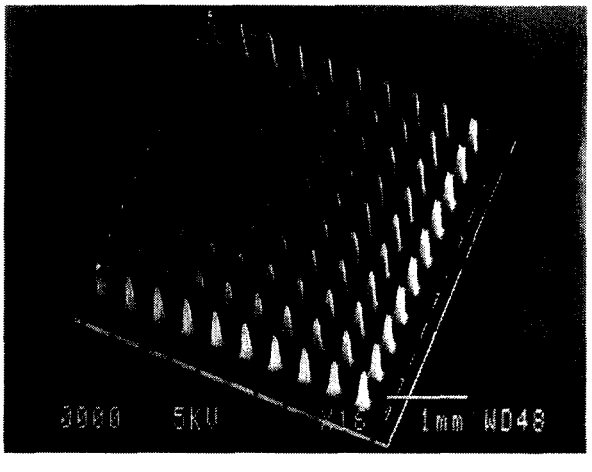

Figure 1. Shown is an SEM micrograph of the MEMS electrode array.

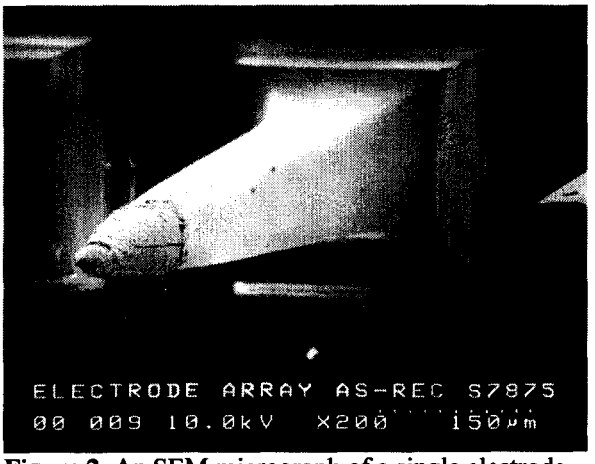

Figure 2. An SEM micrograph of a single electrode is shown. The electrode is made of Si, jacketed in SiN, with PtSi/TiW/Pt at the tip.

Area array flip chip technology is used to attach the electronic chip and the MEMS device. The motivations for using flip chip technology were based in a need to miniaturize, to obtain electrical performance improvements and to accommodate interconnect density demands. Various underbump metallizations were investigated, as well as different interconnect materials. The need for biocompatibility dominated the search for underfills and coatings; however, the fine gap between the chip and the array following bonding did require the use of a low viscosity underfill. As mentioned previously, some specific challenges of the project include (1) handling of the MEMS array in a way that allows reliable soldering of the fine 4 mil joints, without damaging the delicate structures and (2) selection of underfills and coatings capable of isolating the electronics from the body, while maintaining biocompatibility. To ensure the function and form of the commercially purchased electrode array as well as the fully packaged device a thorough, well-defined incoming/ outgoing inspection procedure was developed.

2. Experimental Procedures

2.1 Incoming Inspection

Upon receipt, arrays were inspected using optical microscopy (OM) to insure that there were no large defects and that the overall dimensions of the arrays were as they had been ordered. Following OM, the arrays were examined for mechanical integrity and electrical performance in a Hitachi S4000 Field Emission scanning electron microscope (SEM). A Kevex detector (on an IXRF system) was used for chemical analysis and a sensitive ammeter for monitoring of beam current through each electrode. The arrays were mounted (contact pads down) onto Al studs, using acetone soluble carbon paint, for electrical connection to the SEM stage. The company manufacturing the electrode arrays kindly provided scrap parts to aid in the development of inspection criteria and assembly procedures.

2.2 Assembly

Substrate fabrication: Various substrates were fabricated on 100 mm oxidized Si wafers. Such substrates were used for each of the assemblies discussed in this paper in order to verify attachment methods and design criteria. Evaporated Ti/Pt, Cr/Au and Cr/Ni/Au underbump metallizations were used.

Solder Bumping/Flip chip bonding: Arrays were mounted into the processing holding fixture (Figure 3). Eutectic Sn-Pb solder bumps were then placed on the array pads, using a Packaging Technologies, Inc. ball bumper (Figure 3) with a water-soluble flux. The substrate was then bonded to the bumped array (still located within the holding fixture) using a Semiconductor Equipment Corp. flip chip bonder.

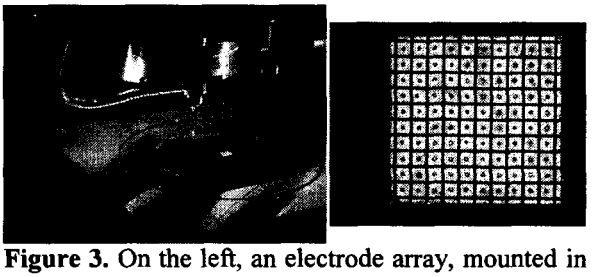

Figure 3. On the left, an electrode array, mounted in the holding fixture, is having solder bumps applied. On the right is an optical micrograph of a bumped electrode array, seated in the holding fixture.

Underfilling/Parylene Coating: A low viscosity FDA approved epoxy is used as the underfill for this assembly. After underfilling, the entire assembly is placed within the Specialty Coatings Systems PDS 1040 Parylene coating system (Parylene C dimer). It should be noted that the array tips cannot be coated and are thus held in polyethylene glycol (PEG) during the coating procedure.

In-Process and Outgoing Inspection: As-soldered electrode array/Si substrate assemblies were observed using OM and SEM, to determine the shape of the solder connection and to make sure that each of the peripheral points were soldered. Electrical continuity was assessed using a standard wafer probing station. Fienfocus X-ray analysis was performed on some of the assemblies. Destructive

testing was performed on selected assemblies. Cross sections were obtained to better assess the solder connections. Following the entire packaging operation, the assembly is inspected for large defects using optical microscopy and it is evaluated for mechanical integrity and electrical function using the SEM.

3. Results and Discussion

3.1 Incoming Inspection and Handling

Inspection of scrap parts provided by the MEMS array manufacturer aided in the development of an incoming inspection criteria for the as-received arrays. Investigators from JPL and the industrial partners worked together to determine the source of different failure modes as well as means of resolving such issues. One of the problems posed during early analysis of parts was a difficulty in soldering some of the Pt bond pads. Although this was not the reason for which these parts were considered scrap, it was a problem nonetheless and had to be taken into account during future operations. In an accompanying experiment, it was found that parts were soldered relatively easily immediately after evaporation/ sputtering, but soldering to such parts became difficult after a few months. Silicone was found to be a possible contaminant; however, no source for contamination was ever found.

The delicate nature of the Si electrodes (Figure 4) complicated the design of the holding fixture. Fragile ledges inhibited the use of mechanical fixtures and processing temperatures reduced the number of viable adhesives. Finally, a fixture was designed to protect the electrodes within a well that was slightly deeper than the 1.5mm long scrap arrays. A "shelf" along the edges of the well protected the ledges and ensured a relatively even bonding surface.

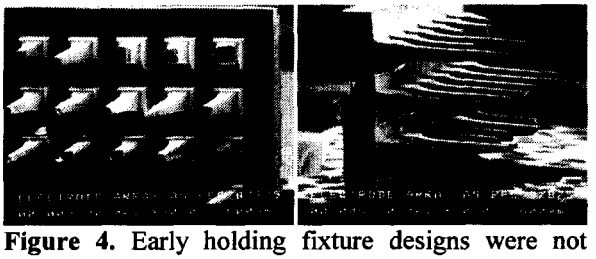

Figure 4. Early holding fixture designs were not successful in protecting the arrays. Above are two SEM micrographs of electrode arrays fractured during processing.

3.2 Assembly

Isotropic Conductive Epoxy: Initially, the electrode arrays were delivered with bond pads that were approximately 290x290μm. Attempts at redefining the bond pads to the 100μm pad size of the electronic chip were unsuccessful. As an alternative, conductive epoxy attachment was attempted. Preliminary tests were performed with epoxy alone. The presence of an uneven epoxy height as well as the lack of any gap between the assembled electrode array and substrate resulted in the use of Au stud bumps (Figure 5).

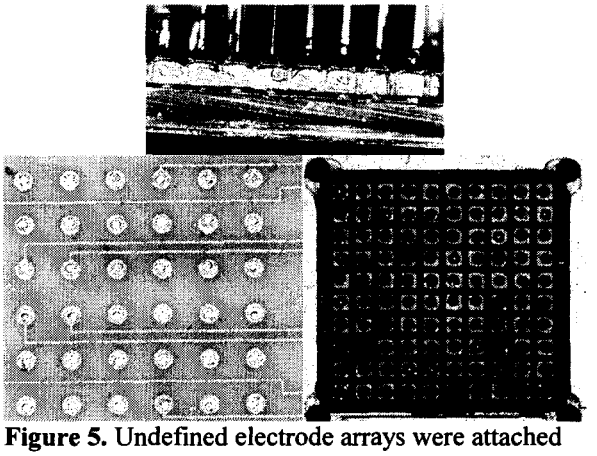

Figure 5. Undefined electrode arrays were attached to the Cr/Au substrate using Ag filled epoxy and Au stud bumps (substrate side).

Solder: Once the manufacturer was able to deliver electrode arrays with 100μm bond pads (Figure 6), soldering experiments were initiated. The first substrate used was Ti/Pt, since these were biocompatible metals used on the electrode array. Although some of the assemblies appeared to be reliably soldered to the substrates (Figure 7), the presence of several opens and the general difficulty soldering to the Pt pads resulted in a change of metallization; Cr/Au was chosen as a replacement.

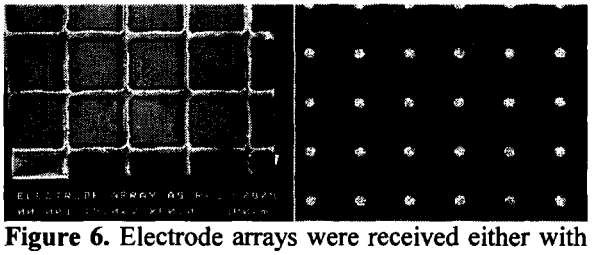

Figure 6. Electrode arrays were received either with 290 x 290μm bond pads (left) or with 100μm diameter pads (right).

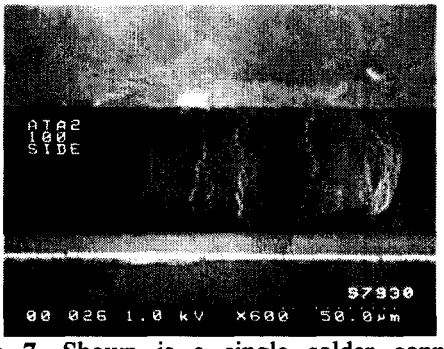

Figure 7. Shown is a single solder connection between an electrode array and a Ti/Pt metallized substrate.

The SEM micrographs in Figures 8 and 9 were taken from as-soldered assemblies between scrap electrode arrays and Cr/Au metallized Si substrates. These substrates were used to optimize soldering parameters (those shown had too great a bonding temperature). Unfortunately, it was found that the bumped die did not always solder to the array bondpads (Figures 10 and 11). In order to solve this problem, the investigators began bumping the electrode array bondpads and flip chip bonding to the substrates (it was clear that there would be no difficulty soldering to the Au on the substrates). In this way the attachment of the solder to the electrode array could be ensured prior to assembly and this issue would no longer be of concern. As an aside, there are two particular things worth noting in Figure 10: (1) the indentation texture of the electrode array bondpads and (2) the slight variation in the size of the solder balls and bonding area.

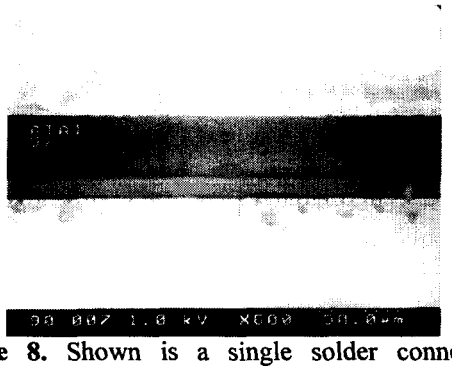

Figure 8. Shown is a single solder connection between an electrode array and a Cr/Au metallized substrate.

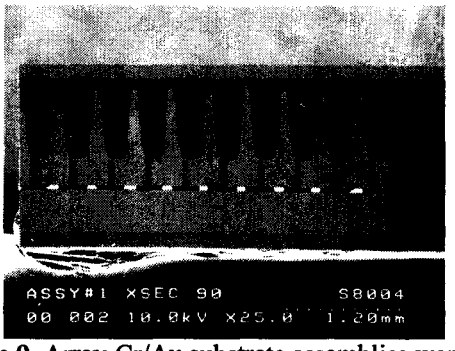

Figure 9. Array-Cr/Au substrate assemblies were cross-sectioned to evaluate the solder joints.

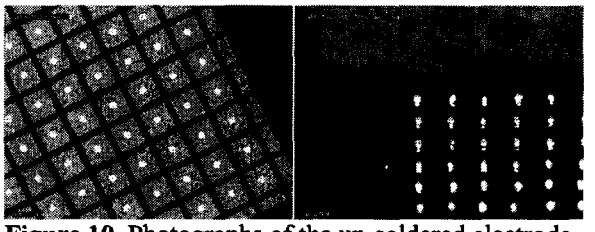

Figure 10. Photographs of the un-soldered electrode array bondpads and bumped substrate are shown.

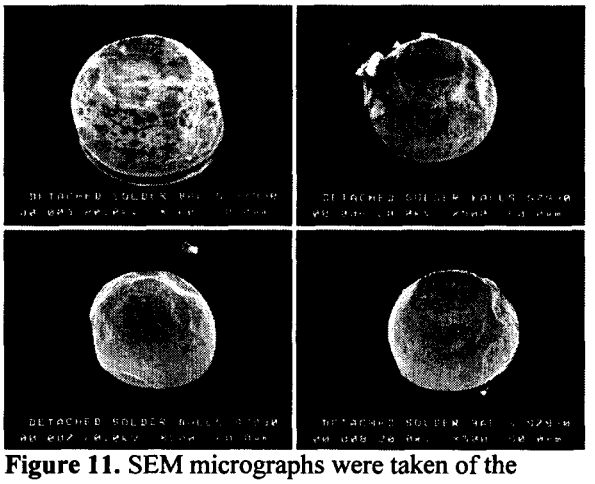

Figure 11. SEM micrographs were taken of the solder bumps on the bumped substrate shown in Figure 10.

Further experimentation using the Cr/Au substrates revealed possible weak points in both the metallization and the electrode array bondpads. A sheared assembly revealed, as shown in Figure 12, revealed that the substrates failed at the Cr/Au interface and the electrode array bondpads failed at the PtSi/TiW interface. It is clear that the eutectic Sn-Pb consumed all of the Au at the interface during soldering, leaving an interface between the solder and the un-solderable Cr layer. As a solution to this problem, a layer of Ni was added between the Cr and Au layers.

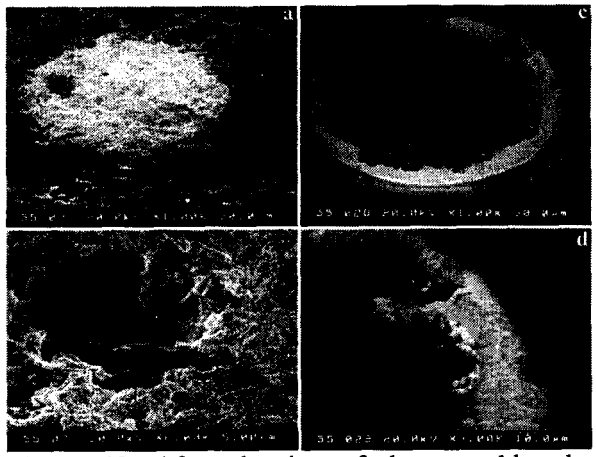

Figure 12. After shearing of the assembly, the electrode array bond pads (a and b) were found to fail at the PtSi/TiW interface, and the substrate (c and d) failed at the Cr/Au interface (eutectic Sn-Pb can be seen along the circumference of the bond pad.

After the underbump metallurgy and soldering parameters were determined (Figure 13), the significant impact of electrode array placement within the holding fixture became apparent. The slight variation in ledge height for the different sides of the electrode array (Figure 14) resulted in a clear misalignment of the electrode array with respect to the substrate (Figure 15). To rectify this issue, the procedure for placement of the electrode array within the holding fixture was changed to ensure that bond pads of the electrode array are flush with the face of the holding fixture.

Underfilling/Parylene Coating: Although Ni and Sn-Pb solder are both incompatible with the biological environment; it is believed that the underfill and coating will be adequate to serve as a barrier between the materials/electronics and the biological environment.

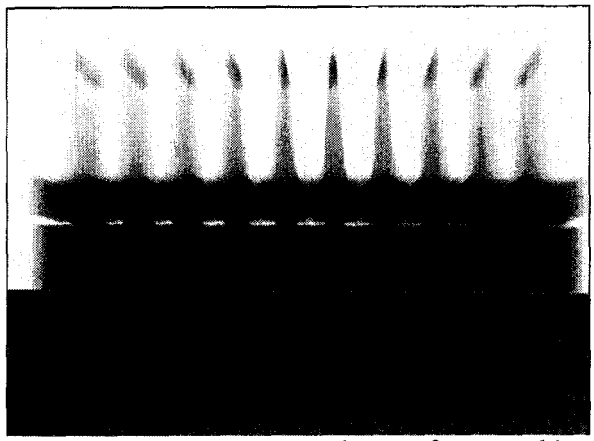

Figure 13. A Feinfocus X-ray image of an assembly following optimization of parameters is exhibited.

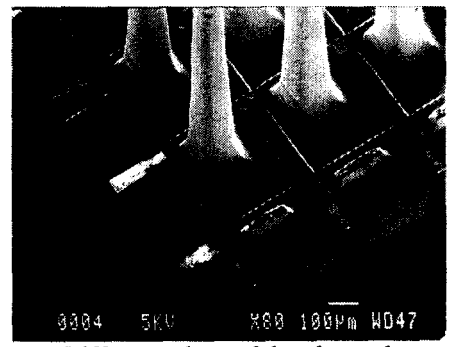

Figure 14. Different edges of the electrode array exhibited various ledge heights.

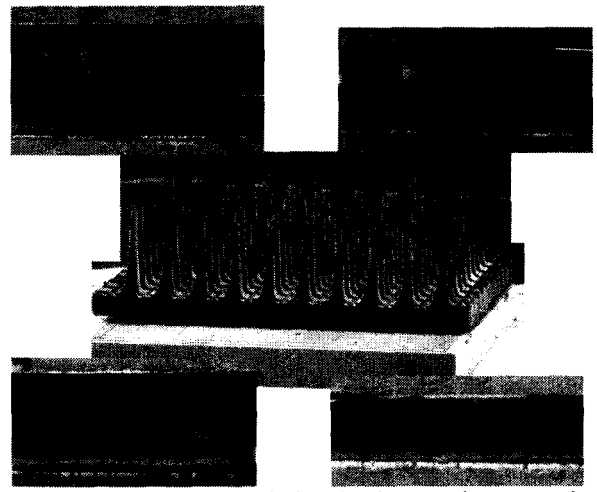

Figure 15. A clear variation in the gap between the electrode array and the substrate, as well as a significantly compressed solder bump in the lower right corner and an unattached solder ball in the upper left corner, were observed for the above assembly.

Since the gap between the electrode array and the substrate is only 50-75µm, it is important to have an underfill with sufficiently low viscosity to fill the gap completely. The first underfill investigated was unable to fill the gap entirely (Figure 16); additionally, the underfill expanded so much during cure that it opened the solder connections in the areas that it did fill (it is worth noting that the solder connection was made between an array and a Ti/Pt substrate). Finally, a low viscosity, FDA approved epoxy was found. In order to further reduce the viscosity of the epoxy, it was heated to 20°C below the curing temperature. It was then allowed to wick up between the two surfaces, completely filling the gap (Figure 17).

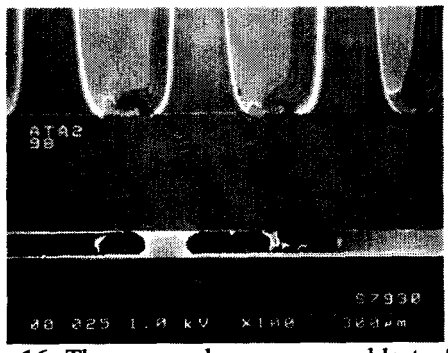

Figure 16. The epoxy shown was unable to fill the gap between the electrode array and the substrate.

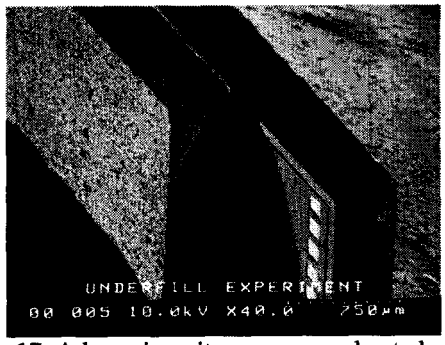

Figure 17. A low viscosity epoxy was heated and allowed to wick up between the gap between two substrates soldered together.

Because of its low absorption of water and capability to conformally coat, as well as the fact that it has been used in medical implants for some time, Parylene was chosen as the final assembly coating. Various methods were used to keep the electrode tips from being coated. The only successful method was the use of PEG, which was allowed to wick up between the electrodes and solidify in place. Several coating experiments were performed in order to optimize parameters (Figure 18).

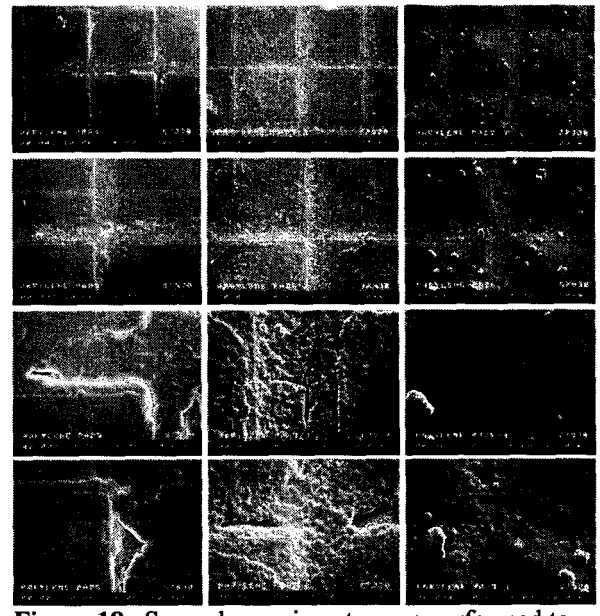

Figure 18. Several experiments were performed to optimize coating and electrode isolation parameters.

Acknowledgement

The work described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.